REMARKS

Reconsideration of the above-identified patent application is requested in view of the remarks that follow.

This reply is responsive to the March 31, 2003, Office Action in this application.

In the March 31, 2003 Office Action, the Examiner rejected claims 68-70, 75 and 76 under 35 U.S.C. 103(a) as being unpatentable over the Igarishi et al. reference in view of the Lin reference and the Tsukamoto reference. Claims 71 and 72 were rejected under 35 U.S.C. 103(a) as being unpatentable over Igarishi et al. in view of Lin and Tsukamoto and further in view of the Kata et al. reference. Claim 73 was rejected under 35 U.S.C. 103(a) as being unpatentable over Igarishi et al. in view of Lin and Tsukamoto and further in view of the Pasch reference. Claim 74 was rejected under 35 U.S.C. 103(a) as being unpatentable over Igarishi et al. in view of Lin and Tsukamoto and further in view of the Knapp et al. reference.

As indicated above, claims 68-76 have been cancelled. New claims 77-85 have been added. Newly-added independent claims 77, 84 and 85 correspond generally to cancelled claims 68, 75 and 76, respectively. Newly-added claims 78-83 correspond generally to cancelled claims 69-74.

With respect to cancelled independent claims 68, 75 and 76, the Examiner states that all of the elements of each these claims are shown primarily by the Igarishi et al. reference. The Examiner cited the Lin reference as showing a device similar to that taught by Igarishi et al. with the interposer matching the coefficient of thermal expansion of the die. The Tsukamoto reference was cited as showing a similar structure where the plate is glass ceramic which matches the coefficient of thermal expansion of the die. It is the Examiner's position that it would have been obvious to use the Tsukamoto material in the Igarishi et al. device for the reason shown by Lin to arrive at the semiconductor integrated circuit wafer scale structure recited in each of claims 68, 75 and 76.

As stated above, independent claims 68, 75 and 76 have been cancelled and new independent claims 77, 84 and 85 have been added. Each of newly-added independent claims 77, 84 and 85 have been amended over their predecessor claims 68, 75 and 76, respectively, to clarify various features of the claimed wafer scale structure for packaging integrated circuits in

order to distinguish the claimed wafer scale structures from the Igarishi et al./Lin/Tsukamoto prior art combination cited by the Examiner.

More specifically, the preamble of each of these newly-added claims has been amended to emphasize that the claim is directed to a wafer scale structure. Moreover, each of the claims has been amended to clarify that the invention, as defined by each of these claims, includes a monolithic substrate of semiconductor material that is subdivided into a plurality of integrated circuit die regions and that each integrated circuit die region includes an integrated circuit formed in that region. As further recited in each of the newly-added independent claims, each of the integrated circuits formed in the plurality of integrated circuit die regions is substantially identical, since, as is well known, each of the circuits is typically formed utilizing a step-and-repeat procedure and an identical mask set.

Additionally, each of independent claims 77, 84 and 85 has been further amended to clarify that the unitary, substantially planar prefabricated solid glass sheet utilized in the claimed wafer scale structure has a plurality of prefabricated hole formed therethrough and that the prefabricated holes are formed to provide a plurality of identical hole patterns, and that each hole pattern is identical to a corresponding pattern of die bond pads of the integrated circuits formed in the substrate wafer.

Each of the claims further recites that an adhesive material disposed between the upper surface of the substrate wafer and the lower surface of the solid glass sheet affixes the solid glass sheet to the wafer substrate such that each pattern of prefabricated holes in the solid glass sheet is aligned with an associated die bond pad pattern included in an associated integrated circuit structure formed in the substrate wafer.

Turning now to the Igarishi et al./Lin/Tsukamoto reference combination cited by the Examiner against independent claims 68, 75 and 76, each of these individual references is directed to a single integrated structure; that is, none of the references discusses structure at an earlier stage of the integrated circuit manufacturing process in which a plurality of integrated circuits are formed in a monolithic substrate wafer semiconductor material that has been subdivided into plurality integrated circuit die regions, wherein each integrated circuit die region includes a substantially identical integrated circuit structure. Furthermore, since none of the references is directed to a wafer scale structure, none of the references either teaches or suggests a unitary, substantially planar prefabricated solid glass sheet having a plurality of prefabricated

hole patterns formed therein so as to provide an association between each of the prefabricated hole patterns formed in the glass sheet and the corresponding conductive die bond pad pattern formed on each of the integrated circuits formed on the substrate wafer.

Essentially, Applicant submits that while each of the Igarishi et al., Lin, and the Tsukamoto references teaches a structure in which electrical connection is made to a pattern of die bond pads, none of the references, consider individually or in combination, either teaches or suggests a wafer scale structures that includes the physical features of a monolithic substrate wafer, a unitary, substantially planar prefabricated solid glass sheet, and an adhesive material disposed between the upper surface of the substrate wafer and the lower surface of the solid glass sheet to affix the solid glass sheet to the wafer to achieve alignment between the prefabricated hole patterns and the glass sheet and the die bond patterns on the semiconductor wafer substrate.

For the reasons set forth above, Applicant submits that each of Applicant's newly-added independent claims 77, 84 and 85 patentably distinguishes over the Igarishi et al./Lin/Tsukamoto reference combination.

Furthermore, since each of newly-added claims 79-83 depends directly from newly-added independent claims 77, Applicant submits that each of dependent claims 79-83 also patenably distinguishes over the cited references.

For the reasons set forth above, Applicant is of the good faith belief that all claims now present in this application patentably distinguish over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

STALLMAN & POLLOCK LLP

Dated: September 26, 2003

By: _____
Michael J. Pollock
Reg. No. 29,098

Attorneys for Applicant(s)

Atty Docket No.: MCSP-101